S/N 08/839,873 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mark R. Thomann et al.	Examiner:	Shelly A. Chase
Serial No.:	08/839,873	Group Art Unit:	2784
Filed:	April 17, 1997	Docket:	303.012US2
Title:	METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM		

FEB 19 1999 PATENT & TRADEMARK OFFICE

AMENDMENT AND RESPONSE

Assistant Commissioner for Patents
Washington, D.C. 20231

FAX RECEIVED
FEB 24 1999
Group 2700

In response to the Office Action of November 16, 1998, please amend the above identified patent application as follows:

IN THE CLAIMS

8. [Once Amended] A method for cyclical redundancy check error generation in a bidirectional system having a cyclical redundancy check generator, a data latch, and a programmable data buffer connected by a plurality of data bus lines, the data latch having a precharge circuit and the data buffer having data buffer outputs programmable to support a plurality of error processing modes, the method comprising the steps of:

inhibiting the cyclical redundancy check generator and the data buffer outputs;

precharging the plurality of data bus lines to a first logic level until a cyclical redundancy check strobe is detected;

turning off the precharge circuit;

activating the data buffer outputs in accordance with one of the plurality of error processing modes corresponding to data stored within the data buffer to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching data on the plurality of data bus lines in the data latch; and

performing a cyclical redundancy check on the ~~data~~ data latched ~~in the data latch,~~ wherein data transferred from the ~~edit~~ data buffer to a first data port is checked for errors and an error check ~~word~~ word is generated for data transferred from the first data port to the ~~edit~~ data buffer.